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or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of $f = 648 \frac{1}{5} = 3.65$ each.

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Communication Systems (VLSICS) Vol.7, No.5/6, December 2016 4 3. CIRCUIT MODEL AND STATIC TIMING ANALYSIS The first step in our design methodology is to classify the logic gates of the circuit according to gate type and no. of inputs such as (AND2, AND3, AND4, OR2, etc.) all these gates are

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